IN THE SPECIFICATION:

In paragraph 15, line 7, please change "NOT" to not.

In paragraph 17, line 4, please change "No change" to "Not set".

In paragraph 17, line 5, please change "No change" to "Not set".

In paragraph 17, line 6, please change "No change" to "Not set".

IN THE CLAIMS:

A Restriction Requirement was specified by the Examiner with Group I including claims 1-15 and Group II including claims 16-33. Applicant hereby makes an election without traverse to prosecute the claims in Group I, claims 1-15.

Please cancel claims 16-33 without prejudice.

Please amend claims 1, 4-6, 9-11, 14, and 15. Unchanged claims are included for the convenience of the Examiner.

1. (Currently Amended) A method, comprising:

setting a memory area used by a bus master device as [non-cacheable] write-through cacheable, the memory and the bus master device being in a computer system;

not setting a bus master status bit (BM_STS) for any [bus master] memory read operation associated with the memory area by the bus master device [with the memory]; and

keeping [placing the] a processor in the computer system [into] in a low power state during the memory read operation.